ID3 THERMAL SWIPE

FINGERPRINT SENSOR

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Revision 1.0

07.06.2017

Revision History

Revision	Date	Description
1.0	07.03.2017	Initial release, from old documents

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Contents

1 Introduction

The id3 Thermal Swipe is a sensor which required no optics, no prism and no light source. It is a single-chip, high-performance, low-cost sensor based on temperature physical effects for fingerprint sensing. The id3 Thermal Swipe has a linear shape, which captures a fingerprint image by sweeping the finger across the sensing area. After capturing several images, id3 proprietary software can reconstruct a full 8-bit fingerprint image. The id3 Thermal Swipe has a small surface combined with CMOS technology, and a Chip-on-Board package assembly. These facts contribute to a low-cost device.
The device delivers a programmable number of images per second, while an integrated analogto- digital converter delivers a digital signal adapted to interfaces such as an EPP parallel port, a USB microcontroller or directly to microprocessors. No frame grabber or glue interface is therefore necessary to send the frames. These facts make the id3 Thermal Swipe an easy device to include in any system for identification or verification applications.

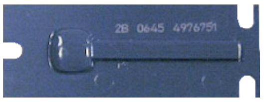


Figure 1: Top view of the sensor

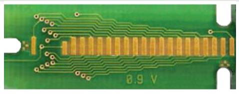
1.1 Features

- Sensitive layer over a 0.35 µm CMOS array
- Image zone: 0.4 x 14 mm = 0.02" x 0.55"
- Image array: 8 x 280 = 2240 pixels
- Pixel pitch: 50 µm x 50 µm = 500 dpi
- Pixel clock: up to 2 MHz enabling up to 1780 frames per second
- Die size: 1.64 x 17.46 mm
- Operating voltage: 3V to 3.6V
- Naturally protected against ESD: > 16 kV air discharge
- Power consumption: 16 mW at 3.3V, 1 MHz, 25℃
- Operating temperature range: -40℃ to +85℃
- RoHS compliant (RoHS Directive)

1.2 Typical applications

- PDA (Access Control, Data Protection)
- Notebook, PC-add on (Access Control, e-business)
- PIN code replacement
- Automated teller machines
- Building access
- Electronic keys
- Portable fingerprint imaging for law enforcement
- TV Access2

1.3 Versions

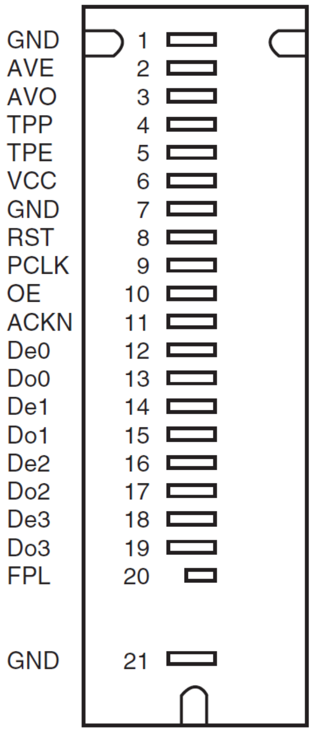
Ref. number	Description	Bottom view
77710001	Chip-On-Board without connector	
77710004	Chip on board with connector	

2 Electrical characteristics

2.1 Pin description

For the 77710001

Pin number	Name	Type
1	GND	GND
2	AVE	Analog output
3	AVO	Analog output
4	TPP	Power
5	TPE	Digital input
6	VCC	Power
7	GND	GND
8	RST	Digital input
9	PCLK	Digital input
10	OE	Digital input
11	ACKN	Digital output
12	De0	Digital output
13	Do0	Digital output
14	De1	Digital output
15	Do1	Digital output
16	De2	Digital output
17	Do2	Digital output
18	De3	Digital output
19	Do3	Digital output
20	FPL	GND
21	GND	GND



The die attach is connected to pins 1, 7 and 21, and must be grounded. The FPL pin must be grounded.

For the 77710004

Pin number	Name	Type
1	GND	GND
2	AVE	Analog output
3	AVO	Analog output
4	TPP	Power
5	TPE	Digital input
6	VCC	Power
7	GND	GND
8	RST	Digital input
9	PCLK	Digital input
10	OE	Digital input
11	ACKN	Digital output
12	De0	Digital output
13	Do0	Digital output
14	De1	Digital output
15	Do1	Digital output
16	De2	Digital output
17	Do2	Digital output
18	De3	Digital output
19	Do3	Digital output
20	FPL	GND
21	GND	GND

2.2 Absolute maximum ratings

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{cc}		GND to 4.6	V
Temperature stabilization power	TPP		GND to 4.6	V
Front plane	FPL		GND to V_{cc} + 0.5	V
Digital input voltage	$RSTPCLK$		GND to V_{cc} + 0.5	V
Storage temperature	T_{stg}		-50 to 95	℃
Lead temperature (soldering, 10 seconds)	T_{leads}	Do not solder	Forbidden	℃

Note: Stresses beyond those listed under “Absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.3 Recommended conditions of use

Parameter	Symbol	Comments	Min	Typ	Max	Unit
Positive supply voltage	V_{cc}		3	3.3	3.6	V
Front plane	FPL	Must be grouded		GND		V
Digital input voltage				CMOS levels		V
Digital output voltage				CMOS levels		V
Digital load	C_L				50	pF
Analog load	C_A R_A	Not connected				pF kΩ
Operating temperature range	T_{amb}	V grade	-40		85	℃
Maximum current on TPP	ITPP		0		100	mA

2.4 Specifications

Resistance

Type	Parameter	Min value	Standard Method
ESD	On pins. HBM (Human Body Model) CMOS I/O	2kV	MIL-STD-883 - method 3015.7
	On die surface (Zapgun). Air discharge	±16kV	NF EN 6100-4-2
Mechanical abrasion	Number of cycles without lubricant multiply by an estimated factor of 20 for correlation with a real finger	200 000	MIL E 12397B
Chemical resistance	Cleaning agent, acid, grease, alcohol, diluted acetone	4 hours	Internal method

Test levels

I	100% production tested at +25℃
II	100% production tested at +25℃, and sample tested at specified temperatures (AC testing done on sample)
III	Sample tested only
IV	Parameter is guaranteed by design and/or characterization testing
V	Parameter is a typical value only
VI	100% production tested at temperature extremes
D	100% probe tested on wafer at T$_{a}mb$ = +25℃

Physical parameter

Parameter	Test level	Min	Typ	Max	Unit

Resolution	IV		50		μm
Size	IV		8x280		pixels
Yield: number of bad pixels	I			5	pixels
Equivalent resistance on TPP pin	I	25	30	45	Ω

Power supply

The following characteristics are applicable to the operating temperature -40℃ $\leq T_a \leq$ 85℃ Typical conditions are: V_{CC} = +3.3 V; T_{amb} = 25℃; FPCLK = 1 MHz; Duty cycle = 50% C_L = 120 pF on digital outputs, analog outputs disconnected unless otherwise specified.

Type	Parameter	Symbol	Test level	Min	Typ	Max	Unit
Power requirements	Positive supply voltage	V_{CC}		3.0	3.3	3.6	V
	Active current on V_{CC} pin, 1MHz Current on V_{CC}, in static mode C_L=0	I_{CC}	I IV		5 4	7 5	mA
	Power dissipation on V_{CC}, C_L=0	P_{CC}	I IV		16 13	28 18	mW
	Current on V_{CC} in NAP mode	I_{CCNAP}	I			10	μA
Analog output	Voltage range	V_{AVX}	IV	0		2.9	V
Digital inputs	Logic compatibility				CMOS		
	Logic "0" voltage	V_{IL}	I	0		0.8	V
	Logic "1" voltage	V_{IH}	I	2.3		V_{CC}	V
	Logic "0" current	I_{IL}	I	-10		0	μA
	Logic "1" current	I_{IH}	I	0		10	μA
	TPE logic "0" voltage	I_{ILTPE}	I	-10		0	μA
	TPE logic "1" voltage	I_{IHTPE}	I	0		300	μA
Digital outputs	Logic compatibility				CMOS		
	Logic "0" voltage (1)	V_{OL}	I	0		0.6	V
	Logic "1" voltage (1)	V_{OH}	I	2.4			V

(1) With $I_{OL} = 1mA$ and $I_{OH} = -1mA$

Timings

Parameter	Symbol	Test level	Min	Typ	Max	Unit
Clock frequency (1)	f_{PCLK}	I	0.5	1	2	MHz
Clock pulse width (high) (1)	t_{HCLK}	I	250			ns
Clock pulse width (low) (1)	t_{LCLK}	I	250			ns
Clock setup time(high)/reset falling edge (1)	t_{Setup}	I			0	ns
No data change(1)	t_{NOOE}	IV	100			ns

Reset pulse width high (1)	t_{HRST}	IV	50			ns
Output delay from PCLK to ACKN rising edge	$t_{PLHACKN}$	I			145	ns
Output delay from PCLK to ACKN falling edge	$t_{PHLACKN}$	I			145	ns
Output delay from PCLK to data output Dxi	t_{PDATA}	I			120	ns
Output delay from PCLK to analog output AVx	$t_{PAVIDEO}$	I			250	ns
Output delay from OE to data high-Z	t_{DATAZ}	IV		34		ns
Output delay from OE to data output	t_{ZDATA}	IV		47		ns

(1) The following characteristics are applicable to the operating temperature -40℃ $\leq T_a \leq$ 85℃ Typical conditions are: nominal voltage; T_{amb} = 25℃; FPCLK = 1 MHz; Duty cycle = 50% C_L = 120 pF on digital outputs, analog outputs disconnected unless otherwise specified.

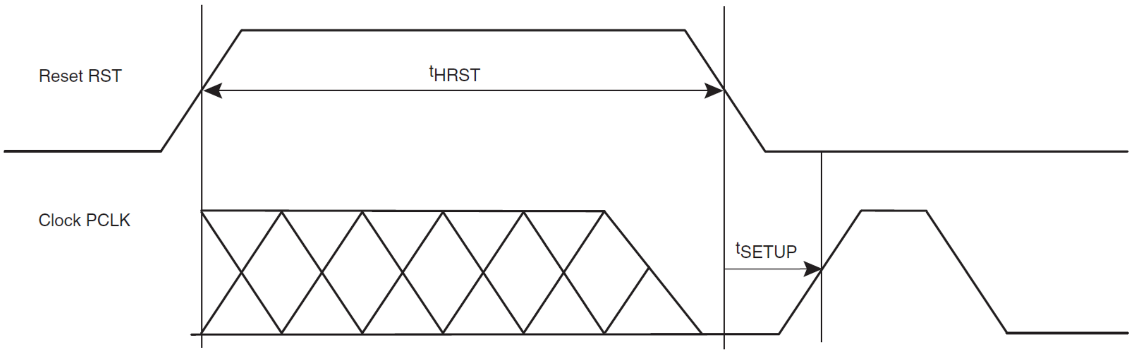


Figure 2: Reset timings

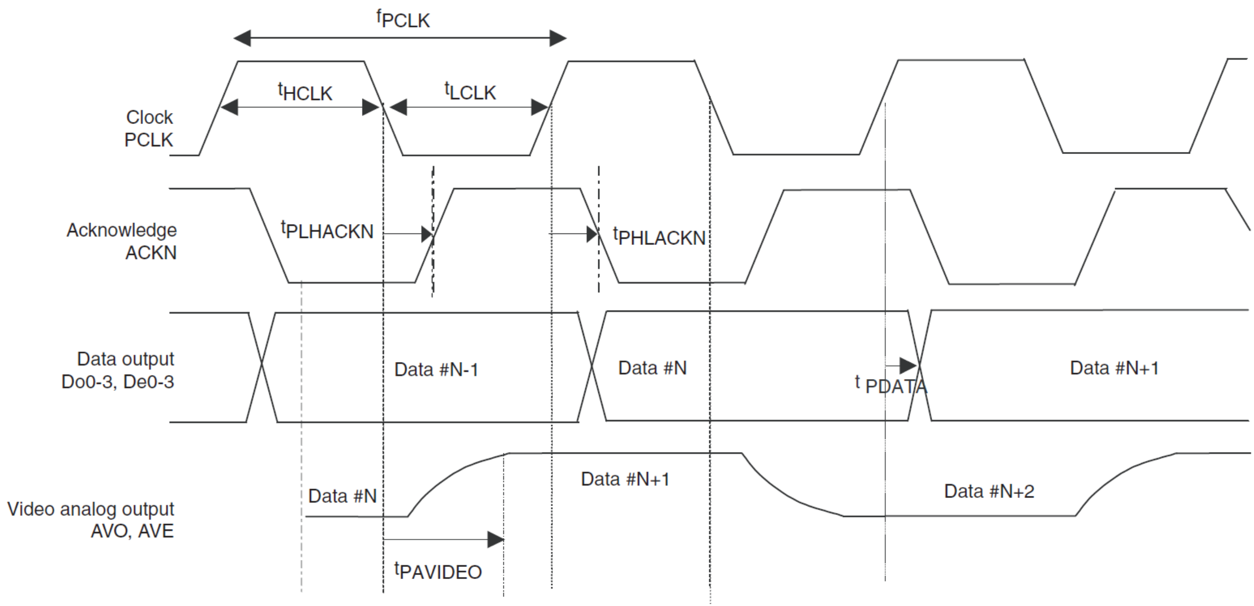


Figure 3: Read one byte/two pixels

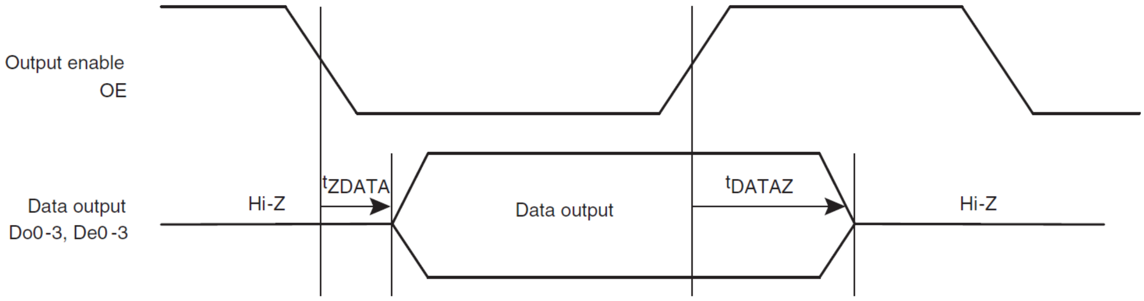


Figure 4: Output Enable

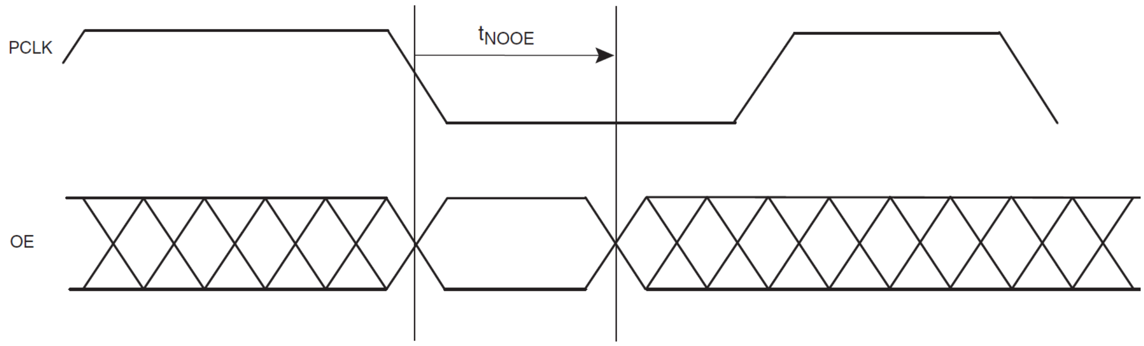


Figure 5: No Data Change

Note : OE must not change during TNOOE after the PCLK falls. This is to ensure that the output drivers of the data are not driving current, so as to reduce the noise level on the power supply.

3 Functional description

3.1 Block diagram

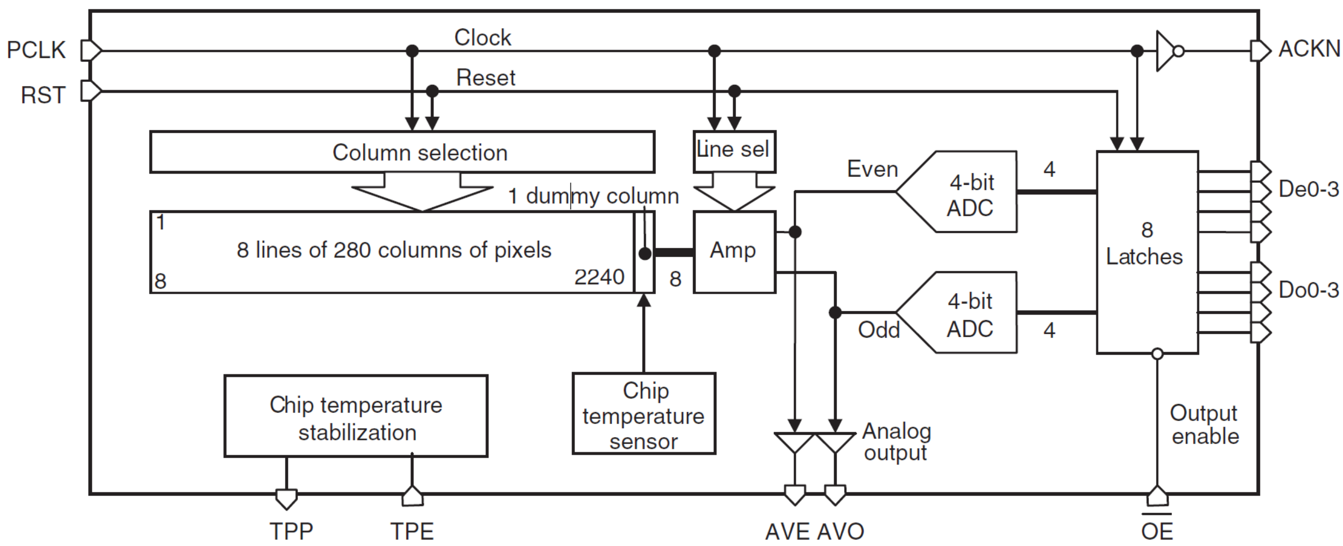


Figure 6: Block diagram of the id3 Thermal Swipe

3.2 General description

The circuit is divided into two main sections: sensor and data conversion. One particular column among 280 plus one is selected in the sensor array (1), then each pixel of the selected column sends its electrical information to the amplifiers (2) [one per line], then two lines at a time are selected (odd and even) so that two particular pixels send their information to the input of two 4-bit analog-to-digital converters (3), so two pixels can be read for each clock pulse.

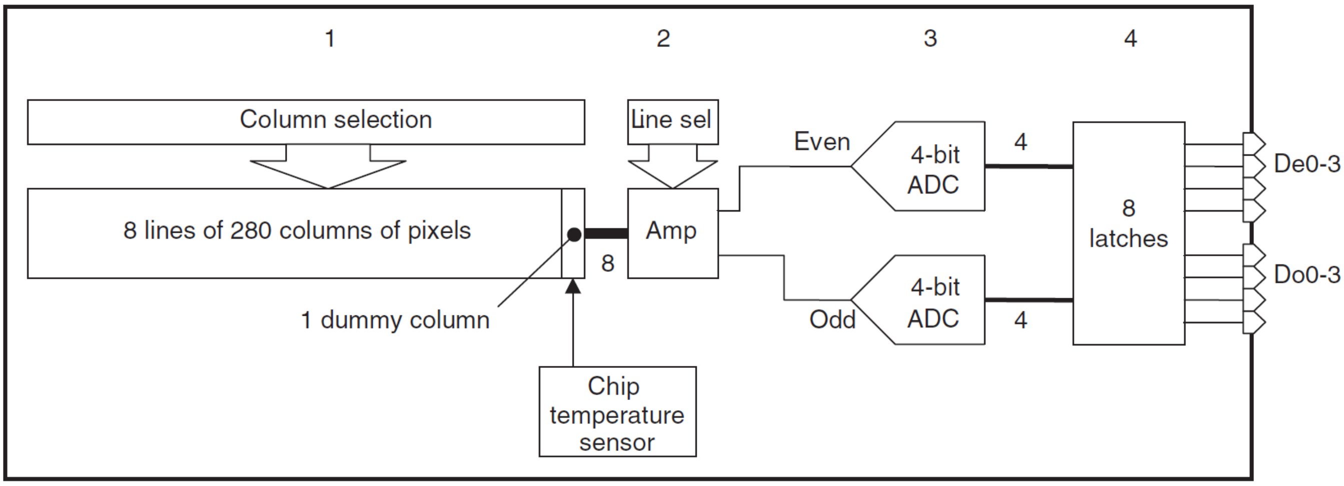


Figure 7: Functional description of the id3 Thermal Swipe

3.3 Sensor

Each pixel is a sensor in itself. The sensor detects a temperature difference between the beginning of an acquisition and the reading of the information: this is the integration time. The integration time begins with a reset of the pixel to a predefined initial state. Note that the integration time reset has nothing to do with the reset of the digital section.
Then, at a rate depending on the sensitivity of the pyroelectric layer, on the temperature variation between the reset and the end of the integration time, and for the duration of the integration time, electrical charges are generated at the pixel level.

3.4 Analog-to-digital converter

An analog-to-digital converter (ADC) is used to convert the analog signal coming from the pixel into digital data that can be used by a processor. As the data rate for the parallel port and the USB is in the range of 1 MB per second, and at least a rate of 500 frames per second is needed to reconstruct the image with a fair sweeping speed of the finger, two 4-bit ADCs have been used to output two pixels at a time on one byte.

3.5 Start sequence

A reset is not necessary between each frame acquisition. The start sequence must consist in:

1. Setting the RST pin to high.
2. Setting the RST pin to low.
3. Sending 4 clock pulses (due to pipe-line).
4. Sending clock pulses to skip the first frame.

Note that after a reset it is recommended to skip the first 200 slices to stabilize the acquisition.

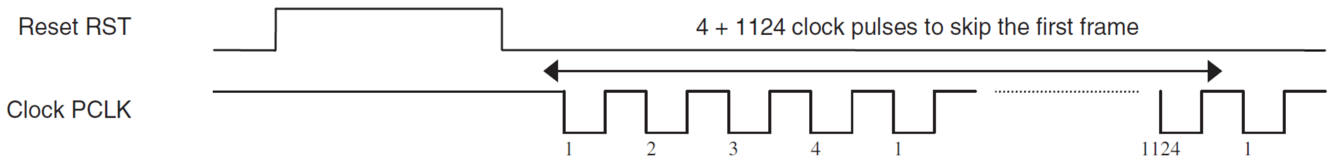


Figure 8: Start sequence

3.6 Reading the frames

A frame consists of 280 true columns plus one dummy column of eight pixels. As two pixels are output at a time, a system must send 281 x 4 = 1124 clock pulses to read one frame. Reset must be low when reading the frames.

3.7 Read one byte/Output enable

The clock is taken into account on its falling edge and data is output on its rising edge. For each clock pulse, after the start sequence, a new byte is output on the Do0-3 and De0-3 pins. This byte contains two pixels: 4-bit on Do0-3 (odd pixels), 4-bit on De0-3 (even pixels). To output the data, the output enable (OE) pin must be low. When OE is high, the Do0-3 and De0-3 pins are in high-impedance state. This facilitates an easy connection to a microprocessor bus without additional circuitry since the data output can be enabled using a chip select signal. Note that the id3 Thermal Swipe sensor always sends data: there is no data exchange to switch to read/write mode.

3.8 Power supply noise

IMPORTANT: When a falling edge is applied on OE (that is when the Output Enable becomes active), then some current is drained from the power supply to drive the eight outputs, producing some noise. It is important to avoid such noise just after the PCLK clock's falling edge, when the pixels' information is evaluated: the timing diagram and time TNOOE define the interval time when the power supply must be as quiet as possible.

3.9 Video output

An analog signal is also available on pins AVE and AVO. Note that video output is available one clock pulse before the corresponding digital output (one clock pipe-line delay for the analog to digital conversion).

3.10 Pixel order

After a reset, pixel 1 is located on the upper left corner, looking at the chip with bond pads to the right. For each column of eight pixels, pixels 1, 3, 5 and 7 are output on odd data Do0-3 pins, and pixels 2, 4, 6 and 8 are output on even data De0-3 pins. The Most Significant Bit (MSB) is bit 3, and the Least Significant Bit is bit 0.

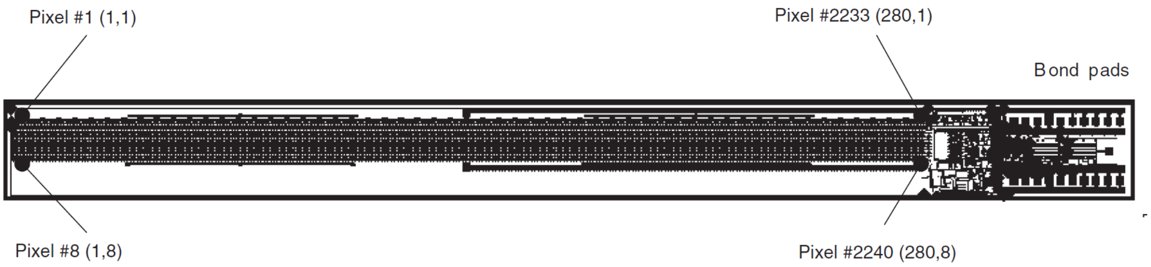


Figure 9: Pixel order

3.11 Synchronization : The dummy column

A dummy column has been added to the sensor to act as a specific pattern to detect the first pixel. Therefore, 280 true columns plus one dummy column are read for each frame.
The four bytes of the dummy column contain a fixed pattern on the first two bytes, and temperature information on the last two bytes.

Dummy byte	Symbol	Odd	Even
Dummy byte 1	DB1	111x	0000
Dummy byte 2	DB2	111x	0000
Dummy byte 3	DB3	rrrr	nnnn
Dummy byte 4	DB4	tttt	pppp

Note : x represents 0 or 1.
The sequence 111X0000 111X0000 appears on every frame (exactly every 1124 clock pulses), so it is an easy pattern to recognize for synchronization purposes.

3.12 Thermometer

The dummy bytes DB3 and DB4 contain some internal temperature information.
The even nibble nnnn in DB3 can be used to measure an increase or decrease of the chip's temperature, using the difference between two measures of the same physical device. The following table gives values in Kelvin.

nnnn decimal	nnnn binary	Temperature differential with code 8 in Kelvin
15	1111	> 11.2
14	1110	8.4
13	1101	7
12	1100	5.6
11	1011	4.2
10	1010	2.8
9	1001	1.4
8	1000	0
7	0111	-1.4
6	0110	-2.8
5	0101	-4.2
4	0100	-5.6
3	0011	-7
2	0010	-8.4
1	0001	-11.2
0	0000	< -16.8

For code 0 and 15, the absolute value is a minimum (saturation).
When the image contrast becomes faint because of a low temperature difference between the finger and the sensor, it is recommended to use the temperature stabilization circuitry to increase the temperature by two codes (that is from 8 to 10), so as to obtain a sensor increase of at least >1.4 Kelvin. This enables enough contrast to obtain a proper fingerprint reconstruction.

3.13 Integration time and clock jitter

The id3 Thermal Swipe is not very sensitive to clock jitters (clock variations). The most important requirement is a regular integration time that ensures the frame reading rate is also as regular as possible, so as to obtain consistent fingerprint slices.
If the integration time is not regular, the contrast can vary from one frame to another.
Note that it is possible to introduce some waiting time between each set of 1124 clock pulses, but the overall time of one frame read must be regular. This waiting time is generally the time needed by the processor to perform some calculation over the frame (to detect the finger, for instance).

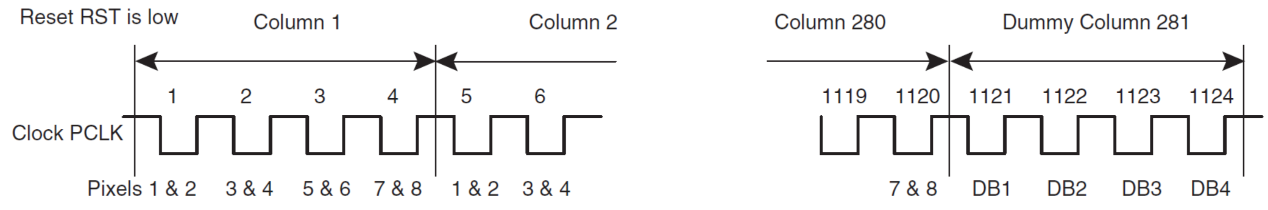


Figure 10: Read one frame

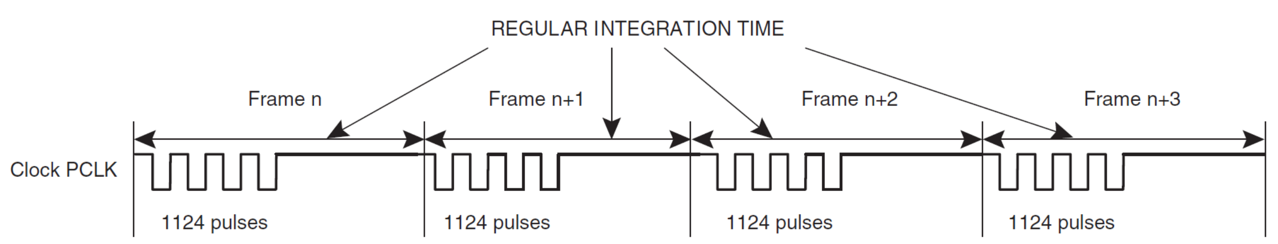


Figure 11: Regular integration time

3.14 Power management and nap mode

Several strategies are possible to reduce power consumption when the device is not in use. The simplest and most efficient is to cut the power supply using external means. A nap mode is also implemented in the id3 Thermal Swipe. To activate this nap mode, you must:

1. Set the reset RST pin to high. By doing this, all analog sections of the device are internally powered down.
2. Set the clock PCLK pin to high (or low), thus stopping the entire digital section.
3. Set the TPE pin to low to stop the temperature stabilization feature.
4. Set the Output Enable OE pin to high, so that the output is forced in HiZ.

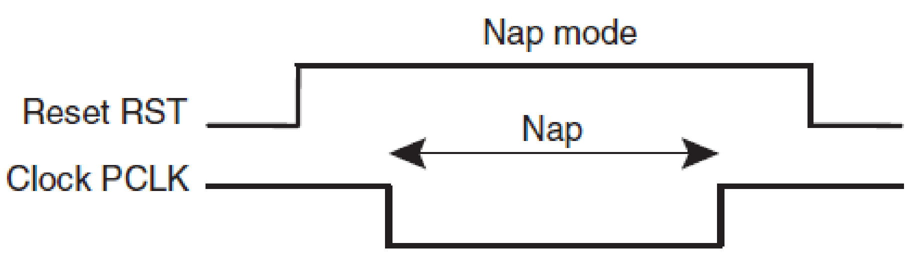


Figure 12: Nap mode

In nap mode,all internal transistors are in shut mode. Only leakage current is drained in the power supply, generally less than the tested value.

3.15 Static current consumption

When the clock is stopped (set to 1) and the reset is low (set to 0), the device's analog sections drain some current, whereas, if the outputs are connected to a standard CMOS input, the digital section does not consume any current (no current is drained in the I/O). In this case the typical current value is 5 mA. This current does not depend on the voltage (it is almost the same from 3 to 3.6V).

3.16 Dynamic current consumption

When the clock is running, the digital sections, and particularly the outputs if they are heavily loaded, consume current. In any case, the current should be less than the testing machine (120 pF load on each I/O), and a maximum of 50 pF is recommended. The id3 Thermal Swipe sensor, running at about 1 MHz, consumes less than 7 mA on the V_{CC} pin.

3.17 Temperature stabilization power consumption (TPP Pin)

When the TPE pin is set to 1, current is drained via the TPP pin. The current is limited by the internal equivalent resistance given and a possible external resistor.
Most of the time, TPE is set to 0 and no current is drained in TPP. When the image contrast becomes low because of a low temperature differential (less than 1 Kelvin), then it is recommended to set TPE to 1 for a short time so that the dissipated power in the chip elevates the temperature, allowing contrast recovery. The necessary time to increase the chip's temperature by one Kelvin depends on the dissipated power, the thermal capacity of the silicon sensor and the thermal resistance between the sensor and its surroundings. As a rule of thumb, dissipating 300 mW in the chip elevates the temperature by 1 Kelvin in one second. With the 30Ω typical value, 300 mW is 3V applied on TPP. If the power supply is 3.6V, an external resistor must be added in the application to limit the current under 100 mA.

4 Mechanical data and packaging

4.1 Product 77710001 (without connector)

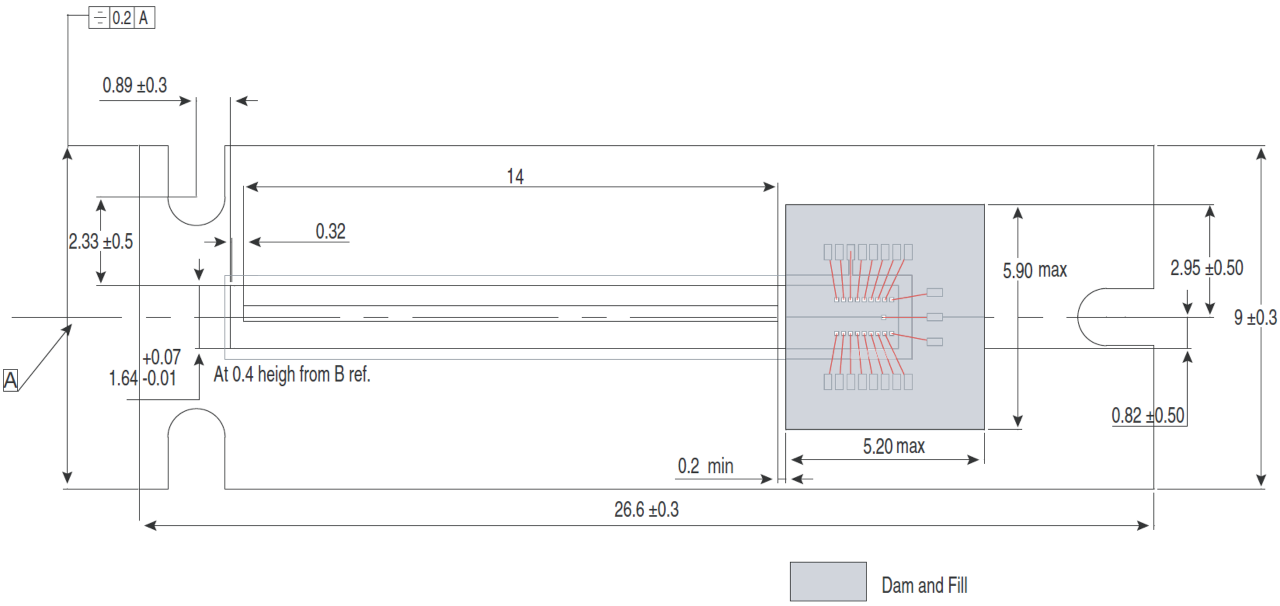


Figure 13: Top view, all dimension in mm

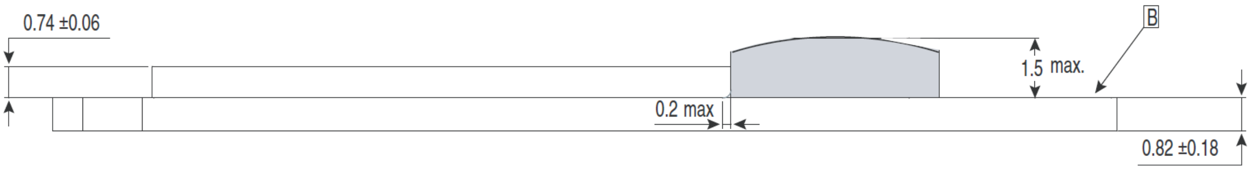


Figure 14: Side view, all dimension in mm

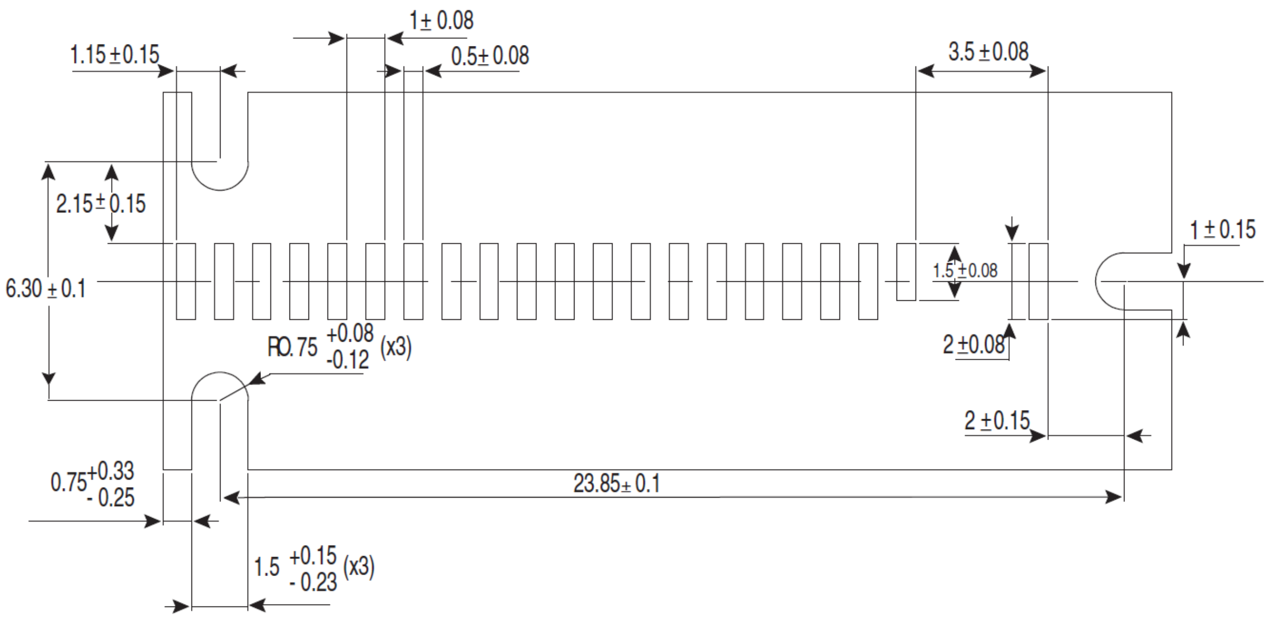


Figure 15: Bottom view, all dimension in mm

4.2 Product 77710004 (with connector)

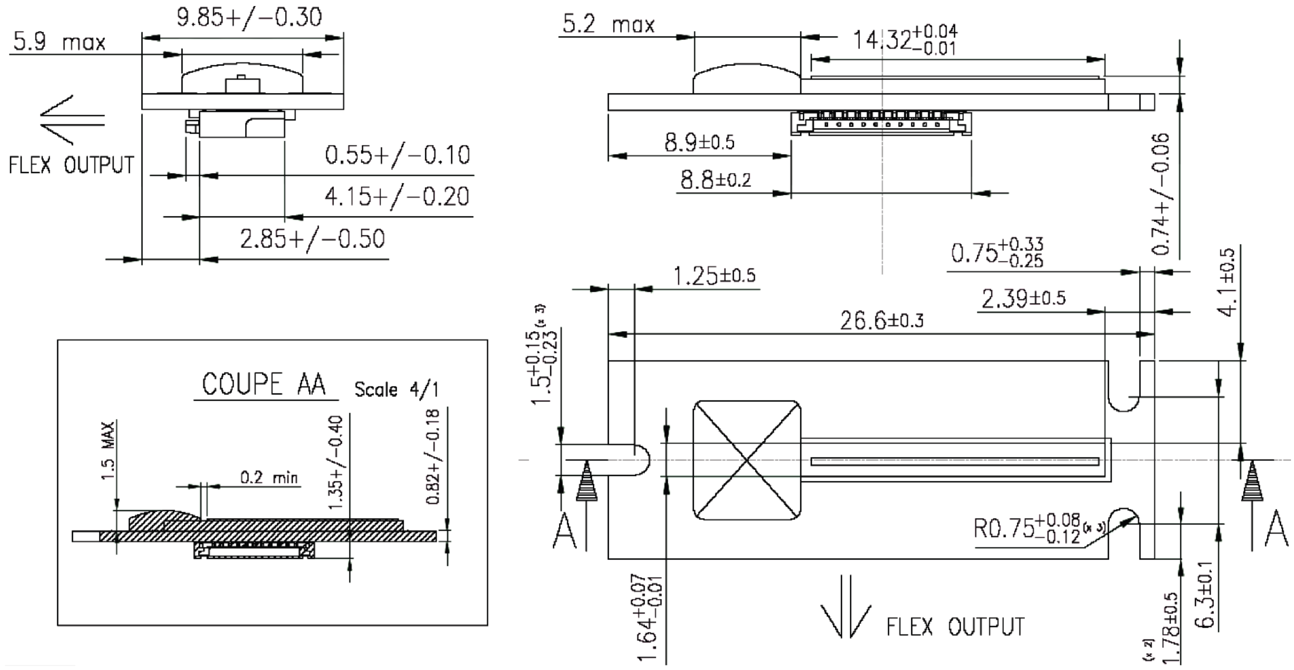


Figure 16: View, all dimension in mm

4.3 Electrical disturbances

When looking at the id3 Thermal Swipe device from the top with the glob top to the right, the right edge must never be in contact with customer casing or any component to avoid electrical disturbances.

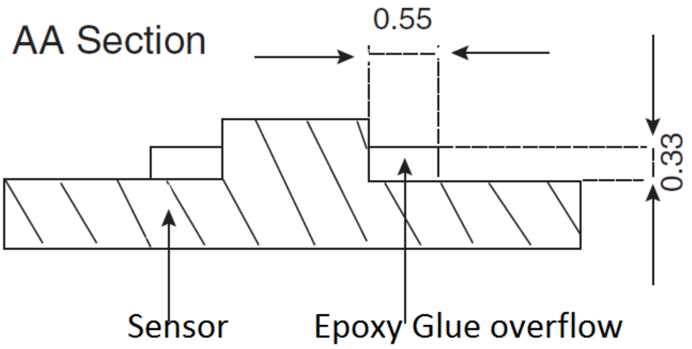


Figure 17: Epoxy overflow

Maximum epoxy overflow width: 0.55 mm on the die edge.

Maximum epoxy overflow thickness: 0.33 mm.

5 Ordering information

Item	Reference
id3 Thermal Swipe sensor without connector	77710001
id3 Thermal Swipe sensor with connector	77710004
id3 Thermal Swipe sensor with connector and flex cable of 50 mm	086U3961
id3 Thermal Swipe sensor with connector and flex cable of 10 0mm	086U3962

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